REMARKS

I. Introduction

With the cancellation without prejudice of claim 23, claims 17 to 22 and 24 to 32 are pending in the present application. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

Applicants thank Examiner for considering the Information Disclosure Statement and for acknowledging the claim for foreign priority and indicating that all certified copies of the priority documents have been received.

II. Objection to the Specification

Regarding the objection to the reference to claims 1 and 16 on page 2, lines 9 to 10 of the Specification, the Examiner will note that this reference was already removed in the Substitute Specification.

Regarding the objection to the second occurrence of the term "switched-on" on page 8, line 7 of the Specification, the Examiner will note that the second occurrence of the term "switched-on" on page 8, line 4 of the Substitute Specification has been changed to --switched-off--. No new matter has been added.

As the objections have been obviated, withdrawal of these objections is respectfully requested.

III. Objection to the Drawings

As regards the objection to the Drawings, the Examiner will note that Figures 1, 2, 3 and 6 have been amended as suggested. No new matter has been added. Accordingly, withdrawal of this objection is respectfully requested.

IV. Rejection of Claims 23 to 30 Under 35 U.S.C. § 112

As regards the rejection of claims 23 to 30 under 35 U.S.C. § 112, second paragraph, for the alleged lack of clarity of the terms "self-blocking" and "self-conducting," the Examiner will note that the Specification has been amended to clarify the above-mentioned terms. Specifically, the phrase "less than or equal to a low operating potential in the case of a self-blocking semiconductor switch" on page 4, lines 13 to 14 of the Specification has been changed to --less than or equal to a

low operating potential in the case of a self-blocking semiconductor switch, i.e., a semiconductor switch that is normally off--, and the phrase "greater than or equal to a high operating potential in the case of a self-conducting semiconductor switch" on page 4, lines 14 to 15 of the Specification has been changed to --greater than or equal to a high operating potential in the case of a self-conducting semiconductor switch, i.e., a semiconductor switch that is normally on--. Accordingly, it is respectfully submitted that claim 23 and its dependent claims 24 to 30 are sufficiently definite.

In view of all of the foregoing, withdrawal of this rejection is respectfully requested.

V. Rejection of Claims 17 to 19 and 32 Under 35 U.S.C. § 102(b) ("Tsuchida et al.")

Claims 17 to 19 and 32 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,545,513 ("Tsuchida et al."). It is respectfully submitted that Tsuchida et al. do not anticipate these claims for at least the following reasons.

Claim 17 relates to a control circuit for controlling an electronic circuit, including: a semiconductor switch; a current path through the semiconductor switch and a line, whereby when the semiconductor switch is switched, an inductance of at least one of the line and a component in the current path produces an excess voltage between a first current-carrying terminal and a second current-carrying terminal of the semiconductor switch; a controllable current source for one of charging and discharging a charge-controlled gate of the semiconductor switch with the aid of a control current; and a control unit controlling the current source in such a manner, that in the case of a switching operation, a terminal voltage across the first current-carrying terminal and the second current-carrying terminal does not exceed a predefined setpoint terminal voltage.

Although Applicants may not agree with the merits of the rejection, to facilitate matters, claim 17 has been amended to incorporate the features of claim 23, claim 23 has been canceled and claim 24 has been amended to change its dependency from claim 23 to claim 17. As an additional note, since claim 23 was rejected as unpatentable over, inter alia, Tsuchida et al., this obviousness rejection will be addressed in this section. Specifically, claim 17 as amended recites, in

relevant part, that ***in a circuit-closing operation, the control unit initially adjusts the setpoint terminal voltage to a first setpoint value, and then to a second setpoint value after expiration of a period of time, the second setpoint value being less than or equal to a low operating potential in the case of a self-blocking semiconductor switch, or greater than or equal to a high operating potential in the case of a self-conducting semiconductor switch***.

Tsuchida et al. do not disclose, or even suggest, that a control unit controls a current source in such a manner, that in the case of a switching operation, a terminal voltage across a first current-carrying terminal and a second current-carrying terminal of a semiconductor switch does not exceed a predefined setpoint terminal voltage. As indicated in column 20, lines 28 to 50 and Figure 9 of Tsuchida et al., V_{GS} of power MOS transistor (101) climbs from zero in the off-state (between times 0 and t1) to ***approximately 5 to 10 V*** in the on-state (between times t2 and t3). Tsuchida et al. make no mention whatsoever of V_{GS} being controlled so as to not exceed a setpoint value when power MOS transistor (101) is switched. In addition, on page 5, lines 17 to 19, the Office Action asserts that "[t]he recited 'setpoint terminal voltage' reads on either of the fixed the voltages set by voltage sources 115 and 116." However, as is clear from Figures 7 and 9 of Tsuchida et al., the voltages $V_t/2$ (V_t is a threshold voltage of power MOS transistor (101)) and 4 V of reference power sources (115) and (116), respectively, are both ***exceeded*** when power MOS transistor (101) is switched on.

Furthermore, Tsuchida et al. do not disclose, or even suggest, that in a circuit-closing operation, a control unit initially adjusts a setpoint terminal voltage of a semiconductor switch to a first setpoint value, and then to a second setpoint value after expiration of a period of time, the second setpoint value being less than or equal to a low operating potential in the case of a self-blocking semiconductor switch, or greater than or equal to a high operating potential in the case of a self-conducting semiconductor switch. ***As discussed above, V_{GS} of power MOS transistor (101) of Tsuchida et al. climbs to approximately 5 to 10 V in an on-state of the transistor, which corresponds to an approximate range and not a specific setpoint value, let alone a second setpoint value***. In addition, regarding the assertion on page 10, lines 16 to 21 of the Office Action, that "[a]s to claims 23 and 24, to the extent understood, these claim limitations also would have been obvious because it is also old and well-known in the art to adjust a set point terminal

voltage during operation of an over voltage protection circuit," Applicants respectfully ***traverse*** and respectfully request published information and/or an affidavit under 37 C.F.R. § 1.104(d)(2) in support of this unsupported allegation. As explained above, and as will be apparent in the proceeding sections of this response, neither Tsuchida et al., nor any other references cited in the rejections of the Office Action disclose or suggest adjusting a setpoint terminal voltage during operation of an over-voltage protection circuit.

Accordingly, it is respectfully submitted that Tsuchida et al. do not anticipate claim 17 for at least the above reasons.

Claim 32 includes features analogous to claim 17 and has been amended in a manner analogous to claim 17. Accordingly, it is respectfully submitted that Tsuchida et al. do not anticipate claim 32 for at least the reasons set forth above.

As for claims 18 and 19, which depend from claim 17 and therefore include all of the features of claim 17, it is respectfully submitted that Tsuchida et al. do not anticipate these dependent claims for at least the reasons set forth above in support of the patentability of claim 17.

In view of all of the foregoing, withdrawal of this rejection is respectfully requested.

VI. Rejection of Claims 17 to 19 and 32 Under 35 U.S.C. § 102(b) ("Glogolja")

Claims 17 to 19 and 32 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,375,074 ("Glogolja"). It is respectfully submitted that Glogolja does not anticipate these claims for at least the following reasons.

Regarding claim 17, Glogolja does not disclose, or even suggest, that in a circuit-closing operation, a control unit initially adjusts a setpoint terminal voltage of a semiconductor switch to a first setpoint value, and then to a second setpoint value after expiration of a period of time, the second setpoint value being less than or equal to a low operating potential in the case of a self-blocking semiconductor switch, or greater than or equal to a high operating potential in the case of a self-conducting semiconductor switch. The circuit shown in Figure 3 of Glogolja includes an output transistor (13), which has a voltage V_{CE} across its collector and emitter, as well as a V_{CE} monitor (47) and a controller (43). The V_{CE} monitor (47) senses V_{CE} of

transistor (13) when the transistor is conducting. If V_{CE} rapidly increases above its saturation level, e.g., due to a short circuit across a load connected to the circuit, the V_{CE} monitor (47) sends a fault signal to the controller (43), and the controller (43) causes the output transistor (13) to turn off. In addition, as indicated in column 4, lines 17 to 33 of Glogolja,

> The V_{CE} monitor 47 can be designed to change the level of fault signal from a low to a high level in the response to the V_{CE} of transistor 13 increasing from a relatively low voltage level to some ***predetermined level***. Usually the predetermined level for triggering the V_{CE} monitor 47 is set close to the saturation voltage level of the transistor being protected, in order to insure the fastest response to the circuit of the transistor going out of saturation from a saturated conduction state. However, as previously indicated, in certain applications it may be desirable to set the predetermined triggering level at some other level than the saturation voltage level of the transistor.

However, neither the controller (43), nor the V_{CE} monitor (47) adjust the above-mentioned predetermined level to a second value after expiration of a period of time. Accordingly, it is respectfully submitted that Glogolja does not anticipate claim 17 for at least these reasons.

Claim 32 includes features analogous to claim 17 and has been amended in a manner analogous to claim 17. Accordingly, it is respectfully submitted that Glogolja does not anticipate claim 32 for at least the reasons set forth above.

As for claims 18 and 19, which depend from claim 17 and therefore include all of the features of claim 17, it is respectfully submitted that Glogolja does not anticipate these dependent claims for at least the reasons set forth above in support of the patentability of claim 17.

In view of all of the foregoing, withdrawal of this rejection is respectfully requested.

VII. Rejection of Claims 17 to 19, 31 and 32 Under 35 U.S.C. § 102(e)

Claims 17 to 19, 31 and 32 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,903,597 ("Tai"). It is respectfully submitted that Tai does not anticipate these claims for at least the following reasons.

Regarding claim 17, Tai does not disclose, or even suggest, that a control unit controls a current source in such a manner, that in the case of a switching operation, a terminal voltage across a first current-carrying terminal and a second current-carrying terminal of a semiconductor switch does not exceed a predefined setpoint terminal voltage. The circuit shown in Figure 2 of Tai includes, inter alia, a switching element (9), whose gate electrode is driven by a square-wave-shaped voltage provided by a voltage source (2). In addition, the principal voltage of the switching element (9) is detected by a voltage detector (7) and is controlled, using a reference signal creation unit (4). ***However, as indicated in column 7, lines 23 to 26 of Tai, the principal voltage of the switching element (9) is only controlled to approximate a voltage reference signal provided by the reference signal creation unit (4), and not controlled so as to not exceed the value of the voltage reference signal***.

Furthermore, Tai does not disclose, or even suggest, that in a circuit-closing operation, a control unit initially adjusts a setpoint terminal voltage of a semiconductor switch to a first setpoint value, and then to a second setpoint value after expiration of a period of time, the second setpoint value being less than or equal to a low operating potential in the case of a self-blocking semiconductor switch, or greater than or equal to a high operating potential in the case of a self-conducting semiconductor switch. As indicated above, the principal voltage of switching element (9) of Tai is controlled to approximate a voltage reference signal provided by reference signal creation unit (4). ***However, Tai makes no mention whatsoever of the voltage reference signal being set to a second value after expiration of a period of time***.

Accordingly, it is respectfully submitted that Tai does not anticipate claim 17 for at least the above reasons.

Claim 32 includes features analogous to claim 17 and has been amended in a manner analogous to claim 17. Accordingly, it is respectfully submitted that Tai does not anticipate claim 32 for at least the reasons set forth above.

As for claims 18, 19 and 31, which depend from claim 17 and therefore include all of the features of claim 17, it is respectfully submitted that Tai does not anticipate these dependent claims for at least the reasons set forth above in support of the patentability of claim 17.

In view of all of the foregoing, withdrawal of this rejection is respectfully requested.

VIII. Rejection of Claim 20 Under 35 U.S.C. § 103(a)

Claim 20 was rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Tsuchida et al., Glogolja or Tai, and U.S. Patent No. 5,373,223 ("Akagi et al."). It is respectfully submitted that the combination of Tsuchida et al., Glogolja or Tai, and Akagi et al. does not render claim 20 unpatentable for at least the following reasons.

Claim 20 ultimately depends from claim 17 and therefore includes all of the features of claim 17. As set forth above, neither Tsuchida et al., nor Tai disclose, or even suggest, all of the features of claim 17, and Glogolja does not disclose, or even suggest, all of the features of claim 17 not disclosed or suggested by Tsuchida et al. and Tai. Furthermore, at the very least, Akagi et al. do not cure the critical deficiencies of Tsuchida et al., Tai and Glogolja with respect to the feature that in a circuit-closing operation, a control unit initially adjusts a setpoint terminal voltage of a semiconductor switch to a first setpoint value, and then to a second setpoint value after expiration of a period of time, the second setpoint value being less than or equal to a low operating potential in the case of a self-blocking semiconductor switch, or greater than or equal to a high operating potential in the case of a self-conducting semiconductor switch. Accordingly, it is respectfully submitted that the combination of Tsuchida et al., Glogolja or Tai, and Akagi et al. does not render unpatentable claim 20, which ultimately depends from claim 17.

In view of all of the foregoing, withdrawal of this rejection is respectfully requested.

IX. Rejection of Claims 21 to 30 Under 35 U.S.C. § 103(a)

Claims 21 to 30 were rejected under 35 U.S.C. § 103(a) as unpatentable over Tsuchida et al., Glogolja or Tai. It is respectfully submitted that neither Tsuchida et al., nor Glogolja, nor Tai render these claims unpatentable for at least the following reasons.

As an initial matter, claim 23 has been canceled, thereby rendering moot the rejection with respect to this claim.

Claims 21, 22 and 24 to 30 ultimately depend from claim 17 and therefore include all of the features of claim 17. As set forth above, neither Tsuchida et al., nor Tai disclose, or even suggest, all of the features of claim 17, and Glogolja does not disclose, or even suggest, all of the features of claim 17 not disclosed or suggested by Tsuchida et al. and Tai. Accordingly, it is respectfully submitted that neither Tsuchida et al., nor Glogolja, nor Tai render unpatentable claims 21, 22 and 24 to 30 for at least these reasons.

In addition, regarding the statements of Official Notice and allegations of well-known fact made with respect to claims 21, 24 and 25 to 30, Applicants respectfully ***traverse*** and respectfully request published information and/or an affidavit under 37 C.F.R. § 1.104(d)(2) in support of these unsupported statements and allegations.

In view of all of the foregoing, withdrawal of this rejection is respectfully requested.

X. Conclusion

In light of the foregoing, Applicants respectfully submit that all pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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